A Study of Volatile and Nonvolatile Static Random Access Memories

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***Abstract*—This paper presents Static Random Access Memory (SRAM), in the volatile and nonvolatile form. The SRAM has been used in the market over a few years because it is trustworthy, durable, and very fast; nevertheless the world's mainstream non-volatile memory, flash memory, needs a new substitute with the same qualities of SRAM. Taking that in consideration it is going to be shown in this work the Magnetic Random Access Memory (MRAM), a nonvolatile memory, in comparison with SRAM, volatile memory, to see how it is similar and efficient. After that, simulations are made upon the volatile SRAM to show the high speed that can be achieved.**

***Index Terms*—Static Random Access Memory, Volatile memory, Non-volatile memory, Magnetic storage, Random-access storage**

I. Introduction

Semiconductor devices include nonvolatile memory devices and volatile memory devices. Nonvolatile memory maintains data stored in a memory cell when power is turned off. The nonvolatile memories may not be suitable to the operations because of the number of data's rewriting required, so it is used volatile ones. However, volatile memories need to be periodically refreshed to maintain the data state [1].

The current mainstream nonvolatile memory, Flash memory, is going to be replaced, but there are a lot of candidates to be the substitute, such as ferroelectric memory (FeRAM) [2], phase change memory (PCM) [3] or magnetoresistive memory (MRAM) [4]. The main difference is in the type of the nonvolatile storage. This paper is going to focus on MRAM, as one of the best candidates to be the next protagonist, comparing the volatile SRAM memory with an MRAM type of nonvolatile SRAM [5].

In this work it is going to be studied the functionality of SRAM and MRAM, making a brief comparison between their behavior and architecture, showing how similar they can be. The MRAM is going to be shown using a 6T bit-cell with 4 Spin-Transfer Torque Magnetic Tunnel Junctions(STT-MTJs) [6], and the SRAM is also going to be shown using a 6T bit-cell [7].

In the Section 2 it is presented a physical architecture explanation. The Section 3 describes the operations of the memories. The section 4 shows the experimental setup. Section 5 concludes the results of the simulations. Section 6 presents the final considerations and future works.

II. SRAM memory architecture

The SRAM memory has a similar architecture in Volatile (SRAM) and nonvolatile (MRAM) type. The main differences are in the bit-cell circuit and the behavior. The nonvolatile that has been studied in this paper has an STT-MTJ. In this section we're going to discuss the main parts of the SRAM memory focusing in the column circuitry [7], with the bit-cell, write driver, a sense amplifier, and the pre-charge.

*1) **Bit-Cell**:* The SRAM bit-cell needs to be able to read, write, and hold the data as long as it is needed. Until the power is turned off in the volatile type and until other data is stored in the nonvolatile. The other SRAM's circuits are just complementary to write or read the stored data in the bit-cell.

a) Volatile: The Volatile bit-cell studied in this article is the 6T Bit-cell, as illustrated in Fig. 2.2, which contains a pair of weak cross-coupled inverters holding the state and a pair of access transistors to read or write the state. If the transistors' supply is turned off the data is lost. [7]

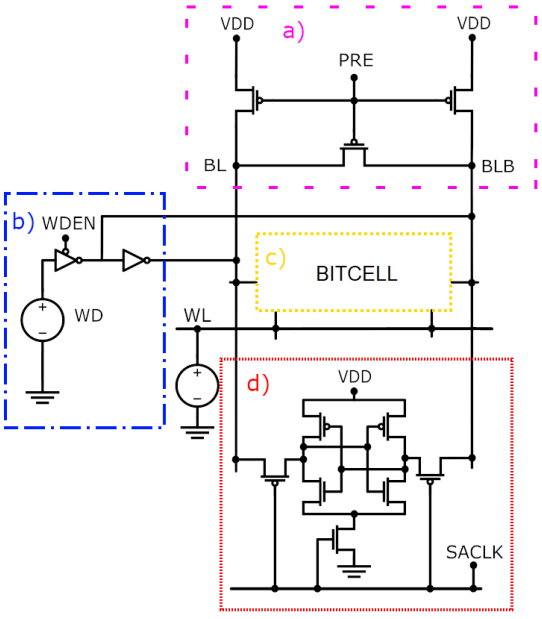

Fig. 1. SRAM Circuit a) Pre-Charge Circuit b) Write-Driver c) Bit-Cel d) Sense Amplifier.

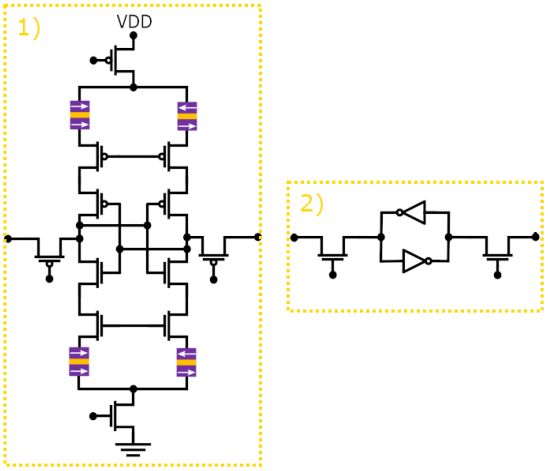

Fig. 2. Types of Bit-cell 1) Nonvolatile Bit-Cell 2) Volatile Bit-Cell

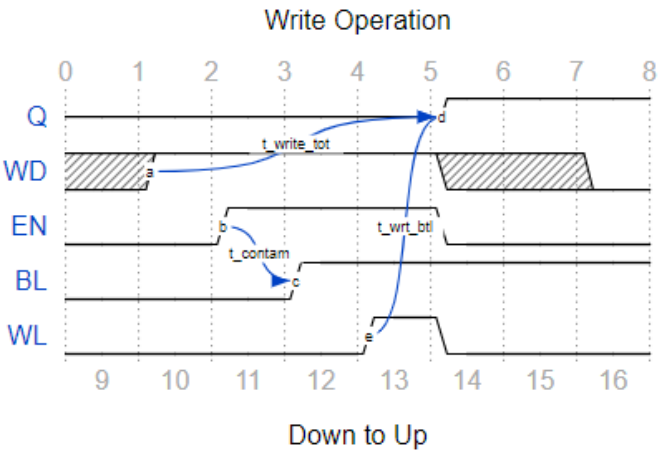

Fig. 3. Write operation diagram. Q - Data stored; WD - Word Data to be written; EN - Tristate Enable signal; BL - Bit-line; WL - Wordline. [9]

b) Nonvolatile: The nonvolatile bit-cell is very similar to the volatile one, but with 4 STT-MTJs(6T4MTJ [6]) connected to the inverters' transistors, as illustrated in Fig. 2.1. To have two pass transistors, connected to the inverters, allow the data to be stored in the volatile and nonvolatile part, and to pass the stored data on the MTJ to the bit-lines.

This bit-cell need to be manipulated by magnetic field to vary the direction of the spins in the MTJs' free layer, changing the value of the resistance and, consequently, the logic value of the output [8].

*2) **Bit-line Pre-Charge**:* The Bit-Line Pre-Charge circuit is presented in Fig. 1a. It is responsible to raise the bit-line to the supply voltage (Vdd) to allow the bit-line to get the data required without disturbing it. [7] The most common implementation is composed of three PMOS transistors.

*3) **Sense Amplifier**:* The Sense Amplifier is responsible for understanding which value is stored into the bit-cell, and it is based on the sense amplifier clock(SACLK). To spend less time getting the value from the volatile bit-cell to the bit-line, the sense amplifier gets a low voltage difference between bit-line(BL) and inverted bit-line(BLB) and enhance this difference to be read by the MUX. In the nonvolatile one, enhance the difference between required bit-cell's voltage and a referenced cell, to get the data's value from the MTJ resistance. [7]

*4) **Write-Driver**:* The Write-Driver as illustrated in the Fig. 1b is used in the write operation, it's responsible to drive to the bit-lines the value that will be written into the bit-cell. Similar to the pre-charge circuit, it will drive the bit-line to the data voltage before the access transistor of the bit-cell is open to writing the data. [7]

III. SRAM MEMORY OPERATION

SRAM memory is used to store data with fast access. It can be in three different conditions: Read, Write, and Hold. These operations are responsible for the memory's management and it needs to have the easiest form to make it as efficient as possible.

*1) **Hold**:* This operation is responsible for maintaining the data into the bit-cell.

a) Volatile: In the volatile memory data is maintained in the pair of weak cross-coupled inverters, as in the Fig. 2.2. This circuit has the data and the complemented data in the input and output of the inverters, maintained by the transistors' supply. It is stored while the supply is turned on, when turned off the data is lost. [7]

b) Nonvolatile: In the nonvolatile memory, the data is maintained by the MTJ, the tunneling magnetoresistance(TMR) effect is the responsible. The MTJs always need to be parallel or antiparallel layers as we can see in the MTJs of the Fig. 2.1. This means different resistances and it is inverted only with a strong magnetic field. The MTJ adopts only two states, until it receives the strong magnetic field it remains in the same state. Because of that the memory stores data while the source is turned off. [8]

*2) **Read operation**:*

a) Volatile: The diagram illustrated in Fig. 4, shows the volatile operation. First, the pre-charge circuit raises the two bit-lines with the same supply voltage. Then open the access transistors by activating the wordline allowing to drive the data to the bit-line from the bit-cell. At the final, the sense amplifier gets the data by the difference between BL and BLB voltage.

b) Nonvolatile: The nonvolatile operation follows the same diagram of the volatile one in Fig. 4, but it is different in the sense amplifier sensing part. It is used to compare the voltage drop rate between the bit-cell and a referenced cell, whose resistance is between the maximum and minimum of an MTJ's resistance, therefore obtaining the data stored.

*3) **Write operation**:*

a) Volatile: The diagram illustrated in Fig. 3 shows write into the volatile memory. It starts with the selection of the data into the write-driver to write into the bit-lines. It activates the enable of the tristate allowing the data pass to the bit-lines and then open the access transistors activating the wordline to contaminate the bit-cell.

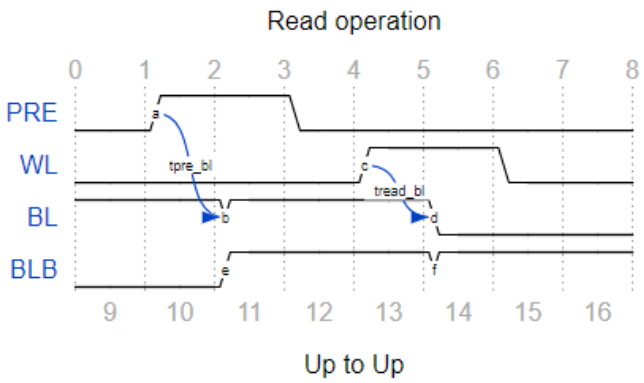

Fig. 4. Read operation diagram. PRE - Pre-charge circuit signal; WL - Wordline; BL - Bit-line; BLB - Bit-line Barred. [9]

b) Nonvolatile: The non-volatile needs to register data into the MTJ. To do this it is necessary to generate a high current that flows through the MTJ. While this current is flowing, it enables the field-line with the data to store. When disabling this current the MTJ will keep the configuration.

IV. Experimental Setup

The results presented compose the first part of the full project, they are focused on the volatile memory. In this section, we present tests that were made on the memories to find the smallest time to read or write into the volatile SRAM.

The tests were made on Cadence's softwares. The circuit netlist were described on SPICE language and the measure algorithm on MDL programming language, these are used to simulate on Candece Spectre.

The measure algorithm uses a *binary search*. The binary search is based on, divide the whole bunch of possibilities into two parts, and then discard the one which does not have the intended value. The limiter of the binary search is based on the difference between BL and BLB or Q and QB, and it is used to find the smallest time. The difference between data '0' and '1' is about 0.8*Vdd.

The tests were made on a SRAM memory(Fig. 1) with: One 6T bit-cell(Fig. 2.2); a write-driver(Fig. 1b); pre-charge circuit(Fig. 1a); a capacitance of 15fF on the bit-lines(BL and BLB). It is used CMOS transistors with 45nm from the library NCSU FreePDK 45nm CMOS technology.

It was tested to all different states of bit-line and bit-cell stored's data, like, 'Down to Up' means ground voltage to supply voltage in the bit-line. All the times are in picoseconds(ps) and it is based on the diagrams of the read operation, Fig. 4, and write operation, Fig. 3. In the Table I the N/A is showed in the cases that the measure algorithm could not be applied because it would result in zero.

A. Write Operation

The write simulation test is based on the write diagram presented on Fig. 3.

The MDL algorithm is used to find the highest start time of EN and WL signal. The final time of the EN is measured by difference on bit-lines on EN signal, depending on the written data. The WL signal is the difference between Q and QB. The results are shown in Table I.

TABLE I
Write Operation Results

Q	Q Low			
Bitline	Down to Down	Down to Up	Up to Up	Up to Down
t_contam(ps)	N/A	325	N/A	328
t_wrt_btl(ps)	N/A	143	142	N/A

Q	Q High			
Bitline	Down to Down	Down to Up	Up to Up	Up to Down
t_contam(ps)	N/A	328	N/A	328
t_wrt_btl(ps)	146	N/A	N/A	146

TABLE II
Read Operation Results

Bitline	Down to Down	Down to Up	Up to Up	Up to Down
Tread_BL(ps)	254	256	256	254
Tpre_BL(ps)	107	108	108	108

B. Read Operation

The read simulation test is based on the reading diagram presented on Fig. 4.

The MDL algorithm is used to find the highest start time of PRE and WL signal. The final time is measured by difference on bit-lines on PRE signal, depending on written data, and in the WL signal is the difference between Q and QB. The results are shown in Table II.

V. Results

The results are presented on Table II and Table I. It is shown the speed of SRAM memory type, doing a read operation (Table II), 350 ps on average and a write operation (Table I) from 140 to 330 ps on average.

The numbers present the reason why SRAM memory is considered a fast volatile memory, the operations into it are at most 460 ps, in the write operation Down to Up.

VI. Final Considerations

In this article, we explained how works an SRAM memory, volatile and nonvolatile, and their operations, proving the high speed of volatile memory (SRAM) with the tests and the importance of a non-volatile memory to the future [5].

In a future work it will be presented tests on a nonvolatile SRAM memory proving it's speed and then implement on an full processor with schematic and layout design.

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REFERENCES

[1] D.-I. Bae, "Memory devices having volatile and non-volatile memory characteristics and methods of operating the same," May 1 2012, uS Patent 8,169,823.

[2] A. Sheikholeslami and P. G. Gulak, "A survey of circuit innovations in ferroelectric random-access memories," *Proceedings of the IEEE*, vol. 88, no. 5, pp. 667–689, 2000. doi: 10.1109/5.849164

[3] H. . P. Wong, S. Raoux, S. Kim, J. Liang, J. P. Reifenberg, B. Rajendran, M. Asheghi, and K. E. Goodson, "Phase change memory," *Proceedings of the IEEE*, vol. 98, no. 12, pp. 2201–2227, 2010. doi: 10.1109/JPROC.2010.2070050

[4] S. Tehrani, J. M. Slaughter, M. Deherrera, B. N. Engel, N. D. Rizzo, J. Salter, M. Durlam, R. W. Dave, J. Janesky, B. Butcher, K. Smith, and G. Grynkewich, "Magnetoresistive random access memory using magnetic tunnel junctions," *Proceedings of the IEEE*, vol. 91, no. 5, pp. 703–714, 2003. doi: 10.1109/JPROC.2003.811804

[5] J. S. Meena, S. M. Sze, U. Chand, and T.-Y. Tseng, "Overview of emerging nonvolatile memory technologies," *Nanoscale research letters*, vol. 9, no. 1, p. 526, 2014. doi: 10.1186/1556-276X-9-526

[6] R. M. Brum, "On the design of hybrid cmos and magnetic memories, with applications to reconfigurable architectures," Ph.D. dissertation, University of Montpellier, Montpellier, France, 2014.

[7] N. Weste and D. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*. Pearson/Addison-Wesley, 2005. ISBN 9780321149015

[8] A. Khvalkovskiy, D. Apalkov, S. Watts, R. Chepulskii, R. Beach, A. Ong, X. Tang, A. Driskill-Smith, W. Butler, P. Visscher *et al.*, "Basic principles of stt-mram cell operation in memory arrays," *Journal of Physics D: Applied Physics*, vol. 46, no. 7, p. 074001, 2013. doi: 10.1088/0022-3727/46/7/074001

[9] "Digital timing diagram everywhere." [Online]. Available: https://wavedrom.com/